REMARKS

In accordance with the foregoing, the abstract, title, specification and claims 1, 2, 5, 17, 23, and 28 are amended. No new matter is presented in any of the foregoing and, accordingly, approval and entry of the amended abstract, title, specification, and claims are respectfully requested

Claims 1-28 are pending and under consideration.

ITEM 2: OBJECTION TO THE SPECIFICATION-ABSTRACT

The Examiner objects to the abstract as containing reference numbers. (Action at page 2). The Abstract is amended herein as suggested by the Examiner. Withdrawal of the objection is requested.

ITEM 2: OBJECTION TO THE SPECIFICATION-TITLE

The Examiner objects to the title as not descriptive. (Action at page 2). The title is amended herein. Applicants submit that the title, as amended, is descriptive and request withdrawal of the objection.

ITEM 5: OBJECTION TO THE SPECIFICATION

The Examiner objects to the specification because of informalities. (Action at page 2). The specification is amended herein as suggested by Examiner, and withdrawal of the objection to the specification is requested.

ITEM 6: OBJECTION TO THE DRAWINGS

The Examiner objects to the drawings contending that FIGs. 9, 13, 14, 16, and 18 include reference numbers not found in the specification. (Action at pages 2-3). The specification is amended herein to include applicable reference signs. Withdrawal of the objection to the drawings is requested.

ITEM 7: OBJECTION TO CLAIM 23

The Examiner objects to claim 23 because of informalities. (Action at page 3). Claim 23 is amended herein as suggested by the Examiner, and withdrawal of the objection to claim 23 is requested.

ITEMS 8-10: REJECTION OF CLAIMS 5, 17, AND 25 UNDER 35 U.S.C. §112

In items 8-10, the Examiner objects to claims 5, 17 and 25 under 35 U.S.C. §112. Claims 5, 17 and 25 are amended herein and Applicants as amended comply with 35 U.S.C. §112. Withdrawal of the rejection to claims 5, 17, and 25 is requested.

TRAVERSE OF 35 U.S.C. §102(b) AND 35 U.S.C. §103(a) REJECTIONS

According to aspects of the present invention, a processor control apparatus includes a first execution processing wherein a plurality of arithmetic units are driven by command sequences from a single command control unit. Thus, a single program counter can be used, and command sequences are input to a plurality of arithmetic logic units so that different commands can be executed concurrently, e.g., a VLIW command. According to an aspect of the present invention, by inputting the same command to each of the arithmetic logic units, an operation equivalent to an SIMD command can be carried out. If separate program counters are provided for a plurality of MIMD commands, respectively, commands handled by the first execution processing are not MIMD commands.

According to an aspect of the present invention, a processor control apparatus includes a second execution processing wherein a plurality of arithmetic units are driven by command sequences, e .g., MIMD commands and program counters are equal in number to the arithmetic units. Thus, according to an aspect of the present invention, switching control between a first execution processing and the second execution processing can be by a command sequence. In the case of the second execution processing, the respective arithmetic units can be associated, or cooperative, with each other (synchronized processing).

Parady (U.S.P. 5,933,627) discusses switching between threads in response to a long-latency event. Parady teaches (See, for example, col. 3, starting at line 26) a method to solve problems that will arise when a plurality of programs are operated in a multi-thread by a processor including a single program counter. Therefore, in Parady, a state of the second execution processing can not be achieved.

Fernando (U.S.P. 6,272,616) discusses a parallel digital processor including a plurality of parallel pipelined paths. Fernando proposes a method to switch between a scalar command (SINGLE), an SIMD command, and an MIMD command. For example, Fig. 5 (See, for example, col. 8, starting at line 16) shows that upon execution of MIMD commands, fetching and arithmetic execution of a SIDE A and a SIDE B are dependent from each other. That is, operations performed by VLIW commands or the like can not be provided.

Dowling (U.S.P. 6,170051) discusses (See, for example, col. 3, starting at line 7) an enhanced VLIW architecture.

An *arguendo* combination of Parady in view of Dowling teaches switching between threads in response to a long-latency event, and an enhanced VLIW architecture.

An *arguendo* combination of Parady in view of Fernando teaches switching between threads in response to a long-latency event including a method to switch between a scalar command (SINGLE), an SIMD command, and an MIMD command.

An *arguendo* combination of Fernando in view of Dowling teaches a method to switch between a scalar command (SINGLE), an SIMD command, and an MIMD command, and an enhanced VLIW architecture.

An *arguendo* combination of Fernando in view of Parady teaches method to switch between a scalar command (SINGLE), an SIMD command, and an MIMD command and switching between threads in response to a long-latency event.

ITEMS 11-19: REJECTION OF CLAIMS 1-6 AND 8 UNDER 35 U.S.C. §102(b) AS ANTICIPATED BY PARADY (U.S.P. 5,933,627)

The Examiner rejects independent claim 1 and claims 2-6 and 8 dependent thereon as anticipated by Parady. (Action at pages 4-7).

As provided in MPEP §706.02 entitled Rejection on Prior Art, anticipation requires that the reference must teach every aspect of a claimed invention. Parady does not support an anticipatory-type rejection by not describing features recited in the present application's independent claims

In contrast to the cited art, independent claim 1 recites a processor control apparatus for controlling a plurality of arithmetic units including a plurality of instruction control units issuing a series of instructions to said plurality of arithmetic units, wherein at least one of said instruction control units being operable to switch between a first execution process driving said plurality of arithmetic units by a single series of instructions and a second execution process driving said plurality of arithmetic units by a plurality of different series of instructions, respectively.

The Examiner contends that these features are described by Parady in that:

> . . . components 150 and 154 teach control units for issuing a series of instructions to said plurality of arithmetic units . . . See the abstract and note that while instructions belonging to a first execution process may be issued from a single instruction control unit, a long latency event (or some other event) within that process will result in switching to driving arithmetic units using a second set of instructions belonging to a second execution process.

(Action at pages 4-5).

Applicants submit however that element 154 are four instruction buffers. (See, Parady, col. 5, line 8). Nothing in Parady discusses that such an instruction buffer is operable to switch between a first execution process driving said plurality of arithmetic units by a single series of instructions and a second execution process driving the arithmetic unit.

Parady merely proposes a method to solve problems that will arise when a plurality of programs are operated in a multi-thread by a processor including a single program counter. Therefore, in Parady, a state of the second execution processing, as recited by independent claims of the in the present invention can not be achieved.

Conclusion

Since features of independent claim 1 and claims 2-8 dependent thereon are not discussed by the cited art, the rejection should be withdrawn and the claims allowed.

ITEMS 20-24: REJECTION OF CLAIMS 1-2 AND 8-9 UNDER 35 U.S.C. §102(b) AS ANTICIPATED BY FERNANDO ET. AL. (U.S.P. 6,272,616)

The Examiner rejects independent claim 1, and claims 2 and 8-9 dependent thereon as anticipated by Fernando. (Action at pages 8-9).

Applicants submit that Fernando does not support an anticipatory-type rejection by not describing features recited in the present application's independent claims

In contrast to the cited art, independent claim 1 recites a processor control apparatus "wherein at least one of said instruction control units being operable to switch between a first execution process driving said plurality of arithmetic units by a single series of instructions and a second execution process driving said plurality of arithmetic units by a plurality of different series of instructions, respectively." Thus, according to aspects of the present invention not only scalar commands (SINGLE), but also VLIM commands (of course, SIMD like operation is possible) and MIMD commands can be performed.

The Examiner contends these features are discussed by Fernando and cites FIG. 1 multiplexer 21 and claim 44. (Action at page 8).

Applicants submit that Fernando does not teach these features, for example, Fernando does not teach that operations performed by VLIW commands or the like can be provided. Fernando merely proposes a method to switch between a scalar command (SINGLE), an SIMD command, and an MIMD command. For example, Fernando's Fig. 5 shows that upon execution of MIMD commands, fetching and arithmetic execution of a SIDE A and a SIDE B are dependent from each other

Applicants further submit that Fernando does not discuss instruction control units being operable to switch between a first execution process driving said plurality of arithmetic units by a single series of instructions. Instead Fernando merely teaches (col. 4, starting at line 20) "processors having any number of parallel instruction pipelines."

Applicants submit that such a parallel arrangement does not describe features as recited

by the present invention.

Conclusion

Since features of independent claim 1 and claims 2 and 8-9 dependent thereon are not discussed by Fernando, the rejection should be withdrawn and claims 1, 2, and 8-9 allowed.

ITEMS 26-27: REJECTION OF CLAIM 7 UNDER 35 U.S.C. §103(a) OVER PARADY IN VIEW OF DOWLING (U.S.P. 6,170,051)

Dependent claim 7 recites a "series of instructions includes a VLIW type instruction."

The Examiner contends that this feature is discussed by Dowling and there is motivation to modify Parady because "when used in conjunction with VLIW instructions, would be utilized more efficiently in order to increase throughput." (Action at page 10).

No Motivation Or Reasonable Expectation of Success Stated Within the Cited Art To Combine In The Manner Proposed By The Examiner

As provided in MPEP §2143 entitled Basic Requirements of a *Prima Facie* Case of Obviousness:

> The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Applicants submit there is no motivation to combine the references in an manner as suggested by the Examiner. Since Parady discusses a switching in response to a long-latency event, Applicants submit there is no motivation for modifying the code therein with VLIW instructions.

Conclusion

Since there is no motivation to modify Parady as suggested by the Examiner, the rejection should be withdrawn and claim 7 allowed.

ITEMS 28-29: REJECTION OF CLAIM 9 UNDER 35 U.S.C. §103(a) OVER PARADY IN VIEW OF FERNANDO

Dependent claim 9 recites a control apparatus including "power control elements for controlling power supply to said arithmetic units based on their instruction executing states."

The Action concedes that this is not taught by Parady. (Action at page 10). Nevertheless, the Examiner contends this is taught by Fernando citing col. 8, lines 10-12.

***Prima Facie* Obviousness Not Established**
Features Not Described By Cited Art Alone Or In Combination

As provided in MPEP §2143.03 "To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F. 2d 1981, (CCPA 1974)."

Applicants submit that Fernando does not teach controlling power supply to arithmetic units based on their instruction executing states. Fernando merely discusses col. 8, lines 10-12 "deactivating processor elements in secondary pipelines which are not needed."

Conclusion

Since *prima facie* obviousness is not established, the rejection should be withdrawn and claim 9 allowed.

ITEMS 30-40: REJECTION OF CLAIMS 10-12, 15-17, 24 and 28 UNDER 35 U.S.C. §103(a) OVER FERNANDO

The Examiner rejects independent claim 10 and claims 11,12 and 15-17 dependent thereon and independent claim 24. The Action concedes that Fernando does not teach a plurality of instruction memories for storing a plurality of series of instructions to be executed by a plurality of arithmetic units. Nevertheless, the Examiner rejects independent claim 10 taking Official Notice is taken that having a plurality of memories for storing independent series of instructions is well known. (Action at page 11).

Examiner's Contentions Unsupported

Applicants respectively submit that the Examiner's contention is unsupported. As understood in the art, such modifications can require code rework and redesign and are not obvious.

As set forth in MPEP §2144.03 Taking of Official Notice Is Unsupported:

> It would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known. For example, assertions of technical facts . . . must always be supported by citation to some reference work recognized as standard in the pertinent art. In re Ahlert, 424 F.2d at 1091, 165 USPQ at 420-21.

Conclusion

Since the taking of Official Notice is unsupported, the rejection should be withdrawn and the claims allowed.

ITEMS 37: REJECTION OF CLAIMS 23, 25, AND 28 UNDER 35 U.S.C. §103(a) OVER FERNANDO

Claim 23 recites a processor including "a plurality of arithmetic units; and a plurality of instruction control units for issuing a series of instructions to drive said arithmetic units in a controlled manner; wherein some of said instruction control units are operable to switch between a first execution process for driving said plurality of arithmetic units by a single series of instructions and a second execution process for driving said plurality of arithmetic units by a plurality of different series of instructions, respectively."

Claim 25 recites a processor including "a selector for selectively switching between a plurality of series of instructions from said instruction memory to be decoded by said instruction decoder, and supplying a series of instructions thus selected to said instruction decoder."

Claim 28 recites a processor controlling method "switching between the predetermined arithmetic units for performing a series of instructions based on the contents of the prescription therein."

The Examiner contends that these features are discussed by Fernando citing component 21.

***Prima Facie* Obviousness Not Established**
Features Not Described By Cited Art

As provided in MPEP §2143.03 "To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F. 2d 1981, (CCPA 1974)."

Applicants submit, however, that Fernando does not discuss instruction control units being operable to switch between a first execution process driving said plurality of arithmetic units by a single series of instructions. Instead Fernando merely teaches (col. 4, starting at line 20) "processors having any number of parallel instruction pipelines."

Conclusion

Since *prima facie* obviousness is not established, the rejection should be withdrawn and claims 23, 25, and 28 allowed.

ITEMS 41-42: REJECTION OF CLAIM 13 U.S.C. §103(a) OVER FERNANDO IN VIEW OF PARADY

Claim 13 recites an instruction queue for temporarily storing, at a stage prior to said selector, a series of instructions to be transmitted from a second one of said instruction memories different from a first one of said instruction memories which stores a series of instructions being executed by said first predetermined arithmetic unit. The Action concedes that this is not discussed by Fernando. (Action at page 17). However the Examiner contends this is taught by Parady and it is obvious to modify Fernando so "instructions are retrieved faster."

No Motivation Or Reasonable Expectation of Success Stated Within the Cited Art To Combine In The Manner Proposed By The Examiner

As provided in MPEP §2143 entitled Basic Requirements of a *Prima Facie* Case of Obviousness:

> The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Applicants submit there is no motivation to combine the references in an manner as suggested by the Examiner. Since Fernando discusses a pipeline including fetch stages to retrieve instructions, Applicants submit there is not a motivation to modify Fernando as the Examiner contends.

Conclusion

Since there is no motivation to combine the cited art, the rejection should be withdrawn and claim 13 allowed.

ITEMS 43-51: REJECTION OF CLAIMS 14 and 19 OVER U.S.C. §103(a) OVER FERNANDO IN VIEW OF DOWLING

The Action concedes that Fernando does not teach a series of instructions including a VLIW. The Examiner contends that Dowling discusses VLIW and there is motivation to modify Fernando with Dowling.

No Motivation Or Reasonable Expectation of Success Stated Within the Cited Art To Combine In The Manner Proposed By The Examiner

As provided in MPEP §2143 entitled Basic Requirements of a *Prima Facie* Case of Obviousness:

> The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Applicants submit there is no motivation to combine the references in an manner as suggested by the Examiner.

Conclusion

Since there is no motivation to combine the cited art, the rejection should be withdrawn and claims 14 and 19 allowed.

ITEMS 43-51: REJECTION OF CLAIM 18, AND 20-21 OVER U.S.C. §103(a) OVER FERNANDO IN VIEW OF DOWLING

The Action concedes that Fernando has not taught an instruction control unit includes a plurality of instruction memories. Nevertheless, the Examiner rejects claim 18 taking Official Notice is taken that having a plurality of memories for storing independent series of instructions is well known. (Action at page 11).

Examiner's Contentions Unsupported

Applicants respectively submit that the Examiner's contention is unsupported. As understood in the art, such modifications can require code rework and redesign and are not obvious.

Conclusion

Since the Examiner's contentions are unsupported, the rejection should be withdrawn and claims 18, and 20-21 allowed.

ITEMS 43-51: REJECTION OF CLAIM 22, AND 26-27 OVER U.S.C. §103(a) OVER FERNANDO IN VIEW OF DOWLING

The Action concedes that Fernando does not discuss arithmetic unit selector for selectively switching between said data generated by said first and second series of instructions being executed and stored in said first and second register files, respectively, according to an instruction from said associated instruction decoder to supply a selected one of said first and second series of instructions to a calculator. However, the Examiner contends that this is taught by Dowling and there is motivation to modify Fernando to reduce complexity.

No Motivation Or Reasonable Expectation of Success Stated Within the Cited Art To Combine In The Manner Proposed By The Examiner

As provided in MPEP §2143 entitled Basic Requirements of a *Prima Facie* Case of Obviousness:

> (t)he teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Applicants submit there is no motivation to combine the references in an manner as suggested by the Examiner and that such a combination would increase complexity.

Conclusion

Since there is no motivation to combine the cited art, the rejection should be withdrawn and claims 22 and 26-27 allowed.

CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: October 18, 2004

By: _____
Paul W. Bobowiec
Registration No. 47,431

1201 New York Avenue, NW, Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501